NOC Reuse for SOC Modular Testing

Pulkit Kumar[1],Navin Kumar agrawal[2]
CCSIT, Teerthanker Mahaveer University, Moradabad
pulkitrajput1998@gmail.com, garg.gla@gmail.com

Abstract—The communication infrasture is the backbone of the NoC system. System on Chip consists of heterogeneous terms of processing engines and unit of memories. An interconnection network provide processing infrastructure. In this paper we are presenting methodology for performance analysis of the Network on Chips (or interconnection Network). It provide memory unit to communicate with high system complexity. It SOC, performance of system depends on ability of the interconnection.

Keywords— Network on Chips (NoC), System on Chips (Soc).

I. INTRODUCTION

A Framework on Chips comprises of numerous motors that coordinate onto similar chips. This Paper we spread proposed test to reuse of this system of reuse noc to execute as Test Access parts in middle based structure. To begin with, the essential reuse system is displayed, including the not very many adjustment actualized in the system between bookings approaches (pre-emptive and non-pre-emptive) are talked about. These fundamental reuse strategies revolve around the importance of express test arranging counts (NoC) designing and channel limit are fixed. The again use of model and booking computations define here expect a flow-like correspondence can be developed, by use of the NoC, between focuses under and outside test sources and map. That doubt recommends a NoC with fixed warrant transmission limit or discussed.

II. SYSTEM ON CHIPS

Integration of multiple cores (e.g. Microprocessor, digital signal processor, RAM, ROM, flash memory, Input/output's components which make a complete system) onto a single chip.

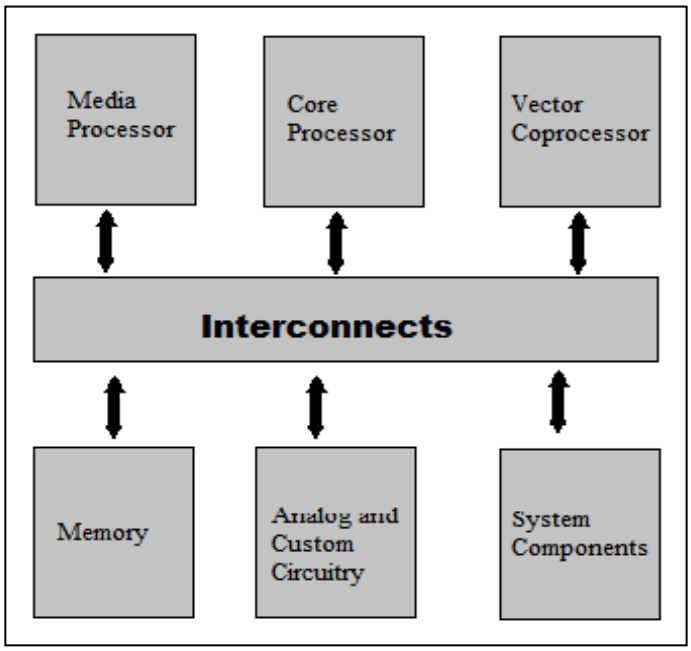


Fig.1 Basic System on chips Model

III. NETWORK ON CHIPS

Testing a NoC-based framework incorporates testing of installed centres Segments and testing of the on-chip organize Testing of implanted centres' is like Trying of inserted centres is like regular SOC testing of on-chip arrange Testing of on-chip arrange .Testing of interconnects, switches/switches input/yield ports switches/switches, input/yield ports, and other component other than the centres.

IV. CORES

Predefined, pre-verified complex blocks, also known as IPs, virtual components

* Processor Cores: ARM, MIPS, IBM PowerPC
* Peripherals: MMU, DMA Controller
* Interface: PCI USB UART
* Multimedia: JPEG compression, MPEG decoder
* Networking: Ethernet Controller, MAC.

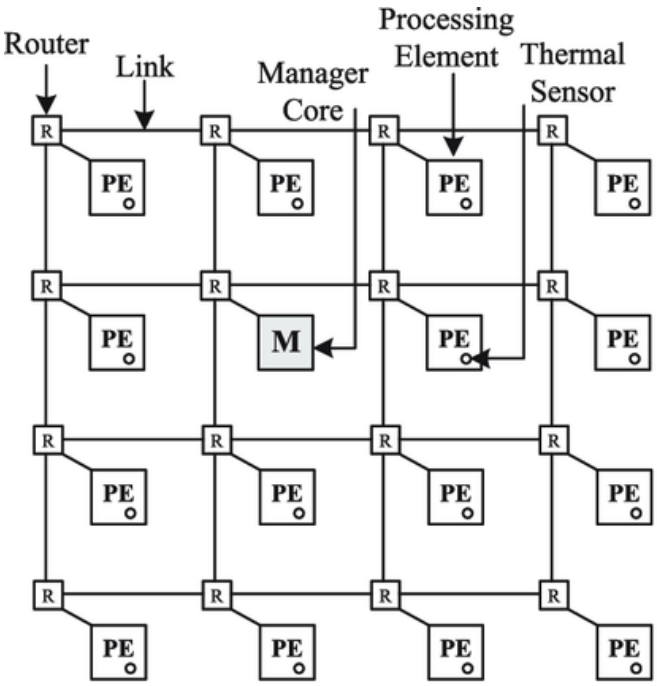


Fig.2 A 4X4 NoC platform

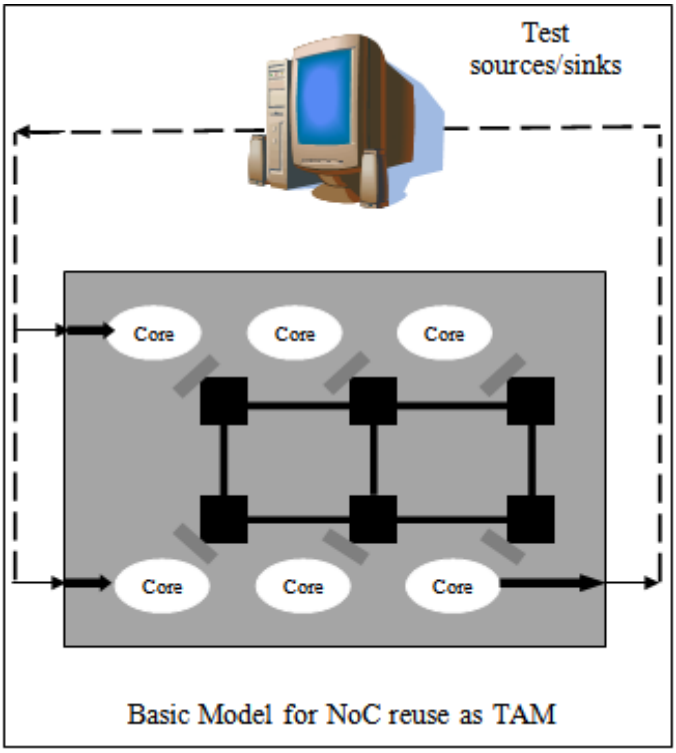
V. NEED FOR NOC FOR SOC MODULAR TESTING

The fundamental need of the NoC reuse For SoC is portrayed test source and map are believed to be off-chip and relationship between them the included focuses is realized by using the on-chip sort out using open pragmatic interface that are related with the NoC.

NoC gives a physical association among all centres associated with it, single can expect that is a way between interface of chip associated with NoC and IP addresses square associated with NoC also. A general test packet structure was apply in first architecture was used in NoC-based.

VI. GENERALLY NOC REUSE MODEL

Plan of again using NoC as check component showed up in first references by Vermeulenet al. They define the NoC reuse for most part for the trial of the NoC itself. General model for Network on chip reuse is depicted in figure.



VII. TAM IMPLEMENTATION

Many TAM implementation have been reported

* Examples
* Multiplexed access
* Reused system bus (AMBA)
* Transparency
* Boundary Scan
* Scalable TAMs (Test bus, Test Rail)
* On one SOC, different TAMs may co-exist.

VIII. NOC REUSE FOR SOC MODULAR TESTING HISTORY

Testing NoC-based framework incorporates testing of inserted centres and testing of the on-chip arrange. Testing of installed centres is like Trying of implanted centres is like regular SOC Testing of on-chip arrange Testing of on-chip organize Testing of interconnects, switches/switches input/yield ports

switches/switches, input/yield ports, and other component other than the centres.

IX. TEST INTERFACE

For Reuse the system to send test information, a test interface must be set up to deal with both practical convention from system and testing application profoundly:

* A wrapper is required for each centre as an interface

X. TEST PACKETS

The network implements a protocol where every message is framed by the header and tail that hold the compulsory information to create the bridge between systems in network. So , to send data test using NoC, a specific architecture of data in the form of packets. A message can be divided into multiple packets for improving performance improving purpose, but mechanisms will follow same rules. For example one can think about solitary message from the test source profoundly, holding all test mechanism of that centre. A straightforward test bundle design was utilized in the first run through in NoC based Test Access Mechanism (TAM) approaches.

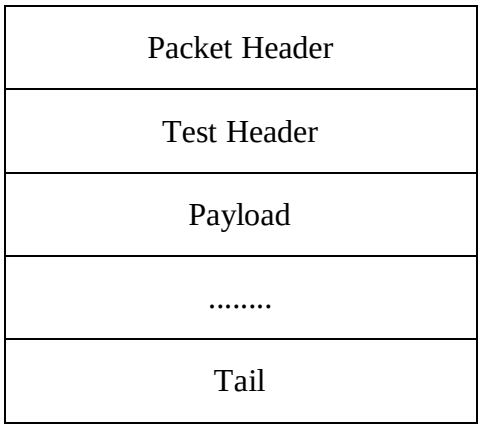


Fig.3 Basic Test Packet Format

XI. NETWORK INTERFACE AND TEST WRAPPER

Centers are associated with the system by methods for a system interface that decipher center correspondence convention to the system convention.

XII. EFFICIENT REUSE OF NETWORK

One test in this reuse-based methodology is that the channel width is dictated by the framework fididhper execution in configuration process and subsequently can't be advanced for test reason

In the substance of system find in NoC test with regards to organize reuse into NoC test, accessible Cap or channel width for wrapper filter chain configuration is controlled by the chain and dictated by the data transmission prerequisites of centres in mode, not only test mode.

The width of channel is predesigned to be 4, and after that half of channel wires will be inert amid centres test while the centres under test just have two sweep chains.

XIII. TEST CHALLENGES

* Hierarchical core reuse
* Need hierarchical test management
* SOC-level test optimization
* Test time can be extremely large
* Need parallel testing or test booking
* Test control must be considered
* Need low-control structure or test planning
* Testable plan robotization
* Need new testable plan devices and stream
* Need new testable plan devices and stream
* Test financial thought
* Need to decide test system and in general test plan

XIV. CONCLUSION

The reuse of embedded processors for test isn't new, yet no past procedure surveyed systems that assistance various processors on a parallel plan. Hanged al. evaluated the reuse of a MIPS processor on a vehicle based plan, while Hwang and Abraham surveyed the reuse of an ARM processor on

Wishbone transport building. Amory et al Built up a PC helped structure mechanical assembly, which urges the originator to arrange fixates on a vehicle based SoC and to create test programs. The results were endorsed completing the structure in FPGA. The second step contains the depiction of the processors reused for test. A processor can be used in the midst of test in different ways. It can run a test program that scrutinizes the compacted test data from a memory, decompresses it and sends it profoundly under test (CUT), or it can fill in as a test structure generator duplicating a pseudo-sporadic BIST reason. All of these test applications must be exhibited in a startling manner. At the present time, we are exhibiting the BIST application, anyway soon we will similarly reinforce decompression.

XV REFERENCES

[1] M. Krishnasamy, Pradeep Kumar Verma, Vivek Mishra, Navin Kumar Agrawal, GarimaMathur, "*A Novel Stochastic Model For Grouped Weighted Multilevel Space-Time Trellis Codes For Rayleigh Fading Channels*" International Journal of Computer Networking, Wireless and Mobile Communications ISSN 2250-1568Vol. 3, Issue 4, Oct 2013, 135-140

[2] Arpitjain, Navin Agarwal, "*Mall Navigation System using wi-fi Router*", proceeding of National Conference on Contemporary Computing by College of Engineering, TeerthankerMahaveer University, Moradabad on MAY 17th 2013.

[3] Navin Kumar Agrawal, Rajeev Kumar and Rahul Rathore "*Impact of Mobile Ad Hoc Networks in e-Governance in*" ,New York Science International Journal ISSN: 1554-0200 , Vol:4 Issue 9,2011,pp83-85.

[4] Navin Kumar Agrawal, Rajeev Kumar and Rahul Rathore "*Solution of 0-1 Programming Problem by using DNA Computing Model",* New York Science International Journal ISSN: 1554-0200, Volume 4 - Number 11,2011,pp10-14.

[5] Hari Om Sharan, Navin Kumar Agrawal Manoj Kumar, Vikas Solanki, "*Solution of Minimum Vertex Cover Problem Using DNA*", to be presented in national Conference held in,Hindustan College of science & Technology Mathura.

[6] Navin Kumar Agrawal,Hari Om Sharan, "*The role of Data Structure in MIS"* to be presented in Inter national Conference held in,GurukulKangriHaridwar.

[7] Navin Kumar Agrawal "*Image transmission on wireless network by using OFDM technology with Rayleigh fading channel*" presented in International Conference held at Institution of Engineers (engineer Bhavan),New Delhi February 2014.

[8] NavinKumaragrawalArpit Jain, "*A Proposed Model for Search Engine Page Ranking Algorithm*" *Proceeding of* System Modeling & Advancement in Research Trends organized by College of Management and Computer applications on October 20-21, 2012.

[9] Navin Kumar Agrawal Arpit Jain, "*Network on Chip Implementation of 2D Mesh Topological Structure in HDL environment*", *Proceeding of* System Modeling & Advancement in Research Trends organized by College of Management and Computer applications on October 20-21, 2012.